NST3946DP6T5G

Dual Complementary General Purpose Transistor

The NST3946DP6T5G device is a spin−off of our popular SOT−23/SOT−323/SOT−563 three−leaded device. It is designed for general purpose amplifier applications and is housed in the SOT−963 six−leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low−power surface mount applications where board space is at a premium.

Features

- h_{FE}, 100−300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- This is a Pb−Free Device

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	40	Vdc
Collector − Base Voltage	V_{CBO}	60	Vdc
Emitter − Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	200	mAdc
Electrostatic Discharge HBM MM	ESD Class	2 B	

THERMAL CHARACTERISTICS

Characteristic (Single Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 1)	P_D	240 1.9	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	520	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 2)	P_D	280 2.2	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	446	°C/W
Characteristic (Dual Heated) (Note 3)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 1)	P_D	350 2.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	357	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 2)	P_D	420 3.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	297	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−4 @ 100 mm^2, 1 oz. copper traces, still air.
2. FR−4 @ 500 mm^2, 1 oz. copper traces, still air.
3. Dual heated values assume total power is sum of two equally powered channels

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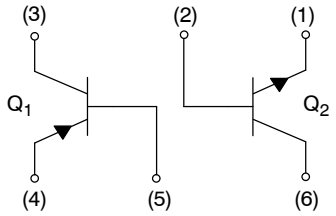
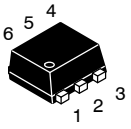


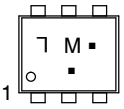
NST3946DP6T5G*

*Q1 PNP
Q2 NPN



SOT−963
CASE 527AD
PLASTIC

MARKING DIAGRAM



L = Device Code
(180° Clockwise Rotation)
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NST3946DP6T5G	SOT−963 (Pb−Free)	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (Note 4)		$V_{(BR)CEO}$			Vdc
(I_C = 1.0 mAdc, I_B = 0)	(NPN)		40	–	
(I_C = −1.0 mAdc, I_B = 0)	(PNP)		−40	–	
Collector – Base Breakdown Voltage		$V_{(BR)CBO}$			Vdc
(I_C = 10 μAdc, I_E = 0)	(NPN)		60	–	
(I_C = −10 μAdc, I_E = 0)	(PNP)		−40	–	
Emitter – Base Breakdown Voltage		$V_{(BR)EBO}$			Vdc
(I_E = 10 μAdc, I_C = 0)	(NPN)		6.0	–	
(I_E = −10 μAdc, I_C = 0)	(PNP)		−5.0	–	
Collector Cutoff Current		I_{CEX}			nAdc
(V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	(NPN)		–	50	
(V_{CE} = −30 Vdc, V_{EB} = −3.0 Vdc)	(PNP)		–	−50	
ON CHARACTERISTICS (Note 4)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	(NPN)		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)			70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			30	–	
(I_C = −0.1 mAdc, V_{CE} = −1.0 Vdc)	(PNP)		60	–	
(I_C = −1.0 mAdc, V_{CE} = −1.0 Vdc)			80	–	
(I_C = −10 mAdc, V_{CE} = −1.0 Vdc)			100	300	
(I_C = −50 mAdc, V_{CE} = −1.0 Vdc)			60	–	
(I_C = −100 mAdc, V_{CE} = −1.0 Vdc)			30	–	
Collector – Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	(NPN)		–	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.3	
(I_C = −10 mAdc, I_B = −1.0 mAdc)	(PNP)		–	−0.25	
(I_C = −50 mAdc, I_B = −5.0 mAdc)			–	−0.4	
Base – Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	(NPN)		0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.95	
(I_C = −10 mAdc, I_B = −1.0 mAdc)	(PNP)		−0.65	−0.85	
(I_C = −50 mAdc, I_B = −5.0 mAdc)			–	−0.95	

4. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	(NPN)		200	−	
(I_C = −10 mAdc, V_{CE} = −20 Vdc, f = 100 MHz)	(PNP)		250	−	
Output Capacitance		C_{obo}			pF
(V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	(NPN)		−	4.0	
(V_{CB} = −5.0 Vdc, I_E = 0, f = 1.0 MHz)	(PNP)		−	4.5	
Input Capacitance		C_{ibo}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	(NPN)		−	8.0	
(V_{EB} = −0.5 Vdc, I_C = 0, f = 1.0 MHz)	(PNP)		−	10.0	
Noise Figure		NF			dB
(V_{CE} = 5.0 Vdc, I_C = 100 μAdc, R_S = 1.0 k Ω, f = 1.0 kHz)	(NPN)		−	5.0	
(V_{CE} = −5.0 Vdc, I_C = −100 μAdc, R_S = 1.0 k Ω, f = 1.0 kHz)	(PNP)		−	4.0	
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = −0.5 Vdc) (NPN) (V_{CC} = −3.0 Vdc, V_{BE} = 0.5 Vdc) (PNP)	t_d	− −	35 35	ns
Rise Time	(I_C = 10 mAdc, I_{B1} = 1.0 mAdc) (NPN) (I_C = −10 mAdc, I_{B1} = −1.0 mAdc) (PNP)	t_r	− −	35 35	
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc) (NPN) (V_{CC} = −3.0 Vdc, I_C = −10 mAdc) (PNP)	t_s	− −	275 250	ns
Fall Time	(I_{B1} = I_{B2} = 1.0 mAdc) (NPN) (I_{B1} = I_{B2} = −1.0 mAdc) (PNP)	t_f	− −	50 50	

NPN TRANSISTOR

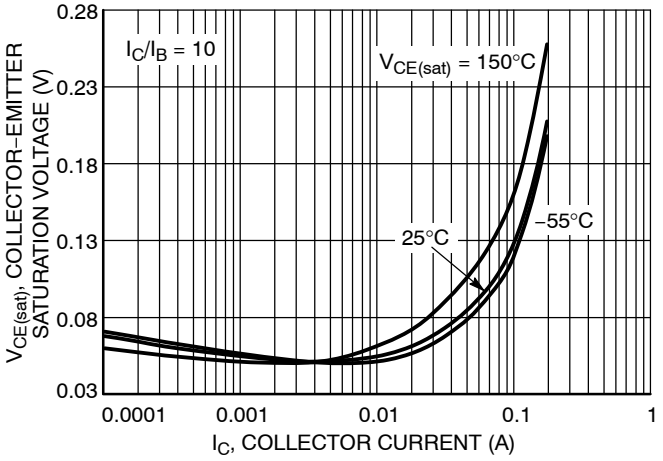


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

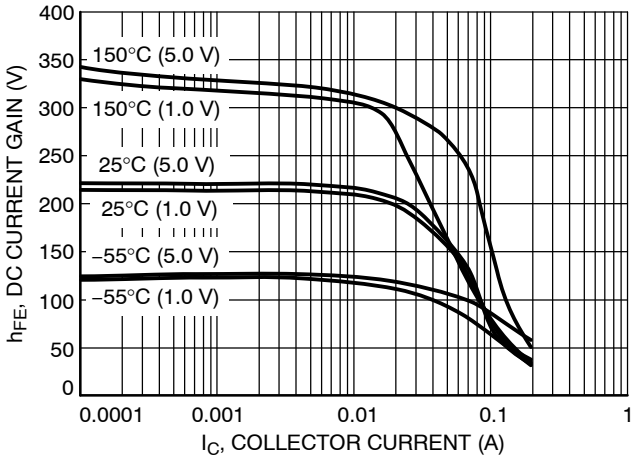


Figure 2. DC Current Gain vs. Collector Current

NPN TRANSISTOR

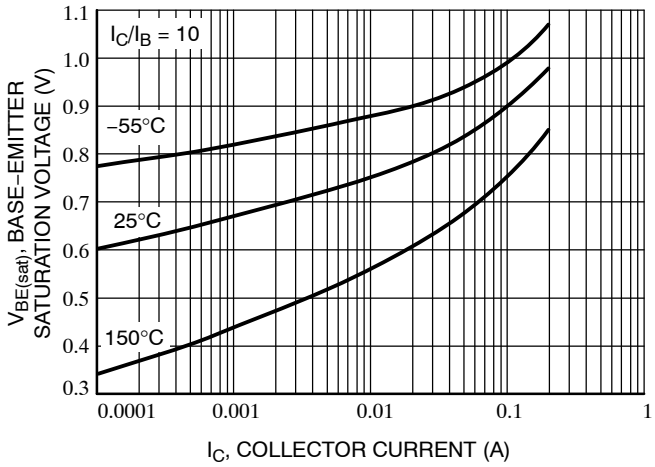


Figure 3. Base Emitter Saturation Voltage vs. Collector Current

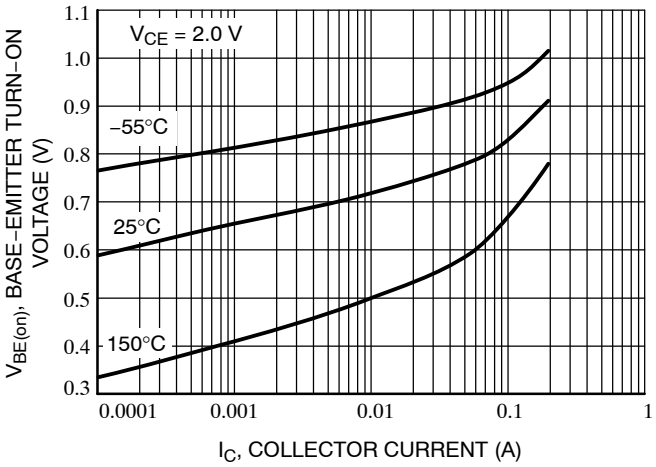


Figure 4. Base Emitter Turn−On Voltage vs. Collector Current

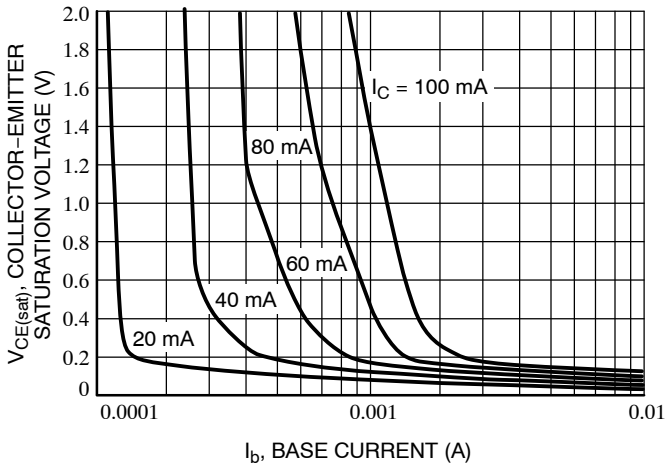


Figure 5. Saturation Region

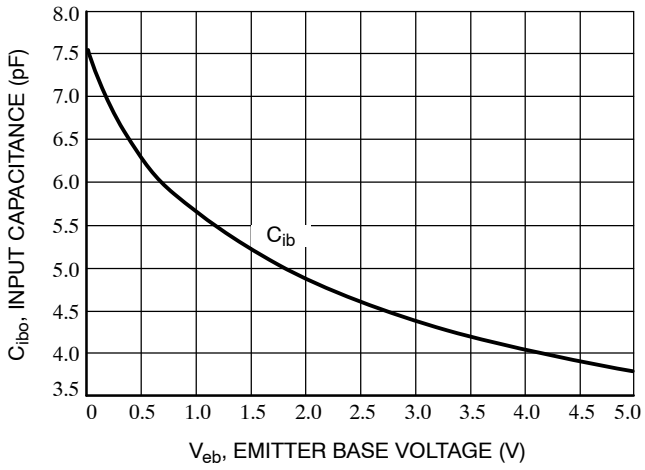


Figure 6. Input Capacitance

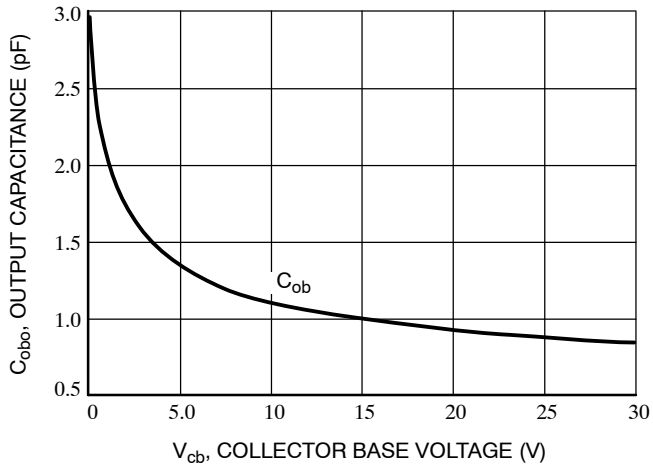


Figure 7. Output Capacitance

PNP TRANSISTOR

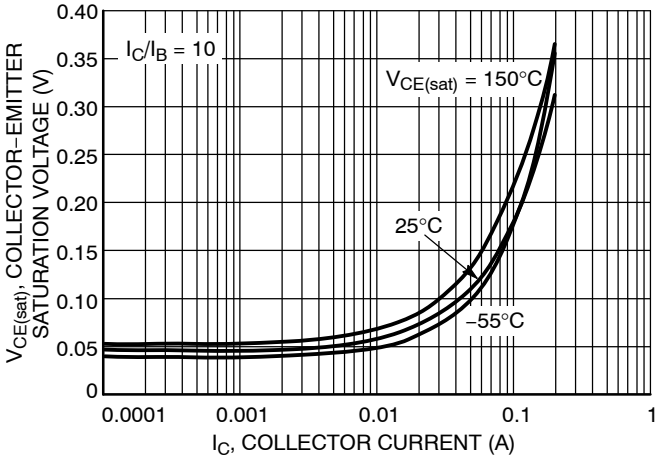


Figure 8. Collector Emitter Saturation Voltage vs. Collector Current

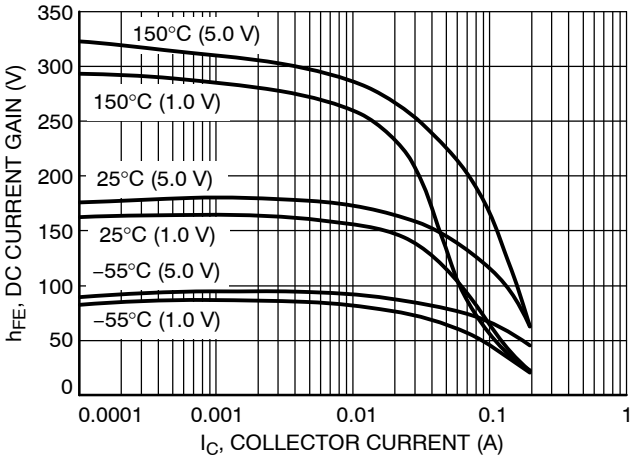


Figure 9. DC Current Gain vs. Collector Current

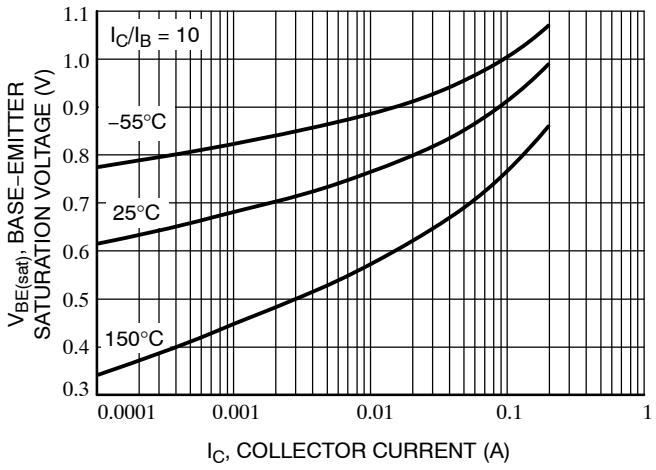


Figure 10. Base Emitter Saturation Voltage vs. Collector Current

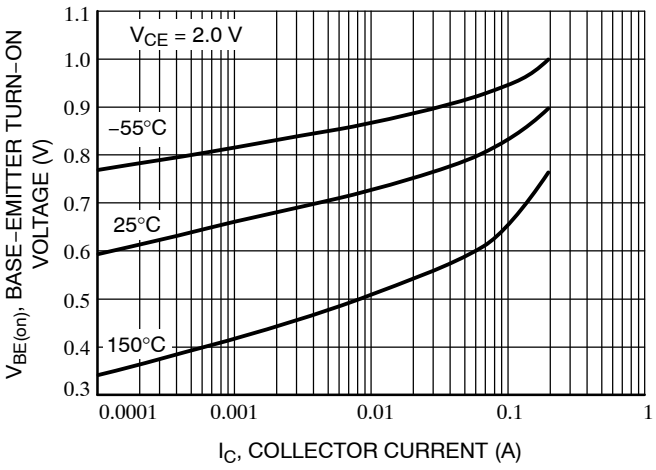


Figure 11. Base Emitter Turn−On Voltage vs. Collector Current

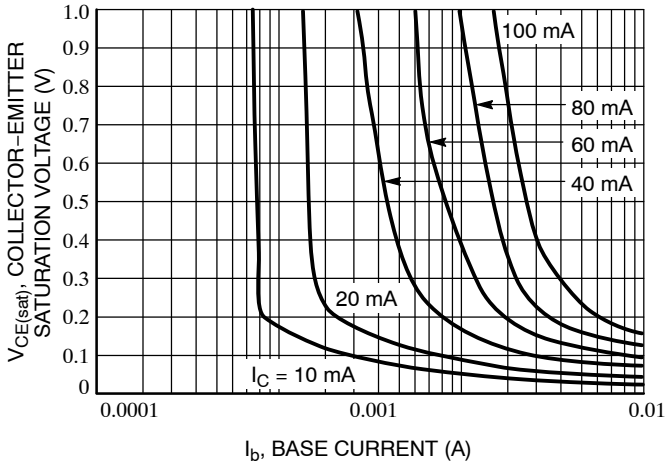


Figure 12. Saturation Region

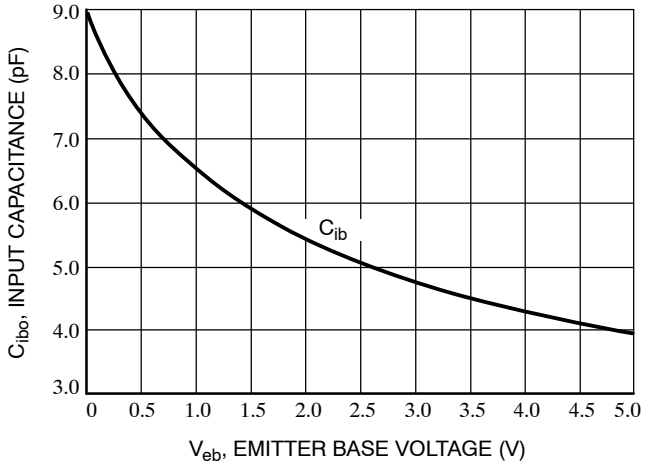


Figure 13. Input Capacitance

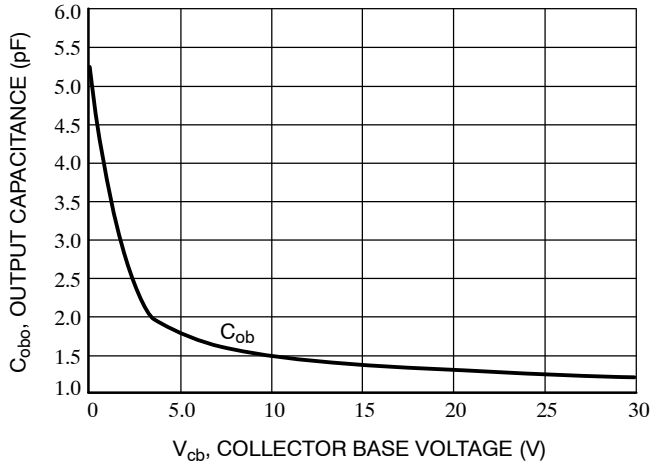
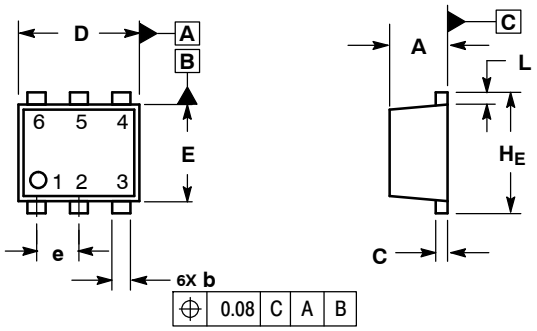


Figure 14. Output Capacitance

NST3946DP6T5G

PACKAGE DIMENSIONS

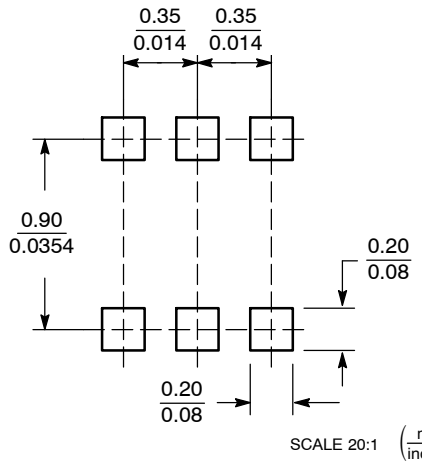
SOT−963
CASE 527AD−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40			
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.07	0.12	0.17	0.003	0.005	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
H_E	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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